Modelling and Implementation of Capacitor to Digital Converters
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Abstract — For capacitive measurement applications different methods were proposed recently. One of the most promising architecture to achieve high resolution is the delta sigma capacitance to digital converter (CDC). It offers a multitude of architectural variants – order of modulator, oversampling ratio, multibit feedback and digital filter functions to design for a requested specification. VHDL-AMS circuit block models were developed to allow for fast simulation and evaluation of different architectures. Implementations have been done for first order, second order and fourth order modulators on a 350nm CMOS technology. For the fourth order modulator a resolution of 52 aF was achieved with an oversampling ratio (OSR) of 50 @ 1 MHz modulator clock and 19.3 aF for the second order modulator with OSR 500 @ 10 MHz modulator clock rate, corresponding to a noise level of 0.2 aF/sqrt(Hz).

Keywords - Capacitive to digital converter (CDC), VHDL-AMS Modelling, Noise analysis,

I. INTRODUCTION

First ideas and implementations about the delta sigma capacitance to digital approach have been done at the institute in the beginning of the 2000 for capacitive moisture and touch sensors. Those early implementations were mostly based on first order modulators and achieved resolutions of some Femtofarads. But they are still good to show the basic principle of the capacitive to digital converter. Recently we developed a VHDL-AMS-Model Library to enable us to simulate and evaluate different architectures very efficiently. Based on the first order modulator, a contactless obstacle detection system for automatic operated windows and doors has been implemented.

Figure 1 shows a block diagram of a first order capacitance to digital modulator in switched capacitor technology. The basic idea is, to operate the modulator with a reference voltage at the analogue input and to use the input charge capacitor as capacitive sensor. Beside the oversampling and noise forming behaviour of the modulator this approach also shows a big advantage of an easy offset compensation by adding a second input branch in parallel to the sensor branch subtracting a fixed charge from the input signal. Gain setting is also easily achieved by implementing different capacitors in the feedback, which can be selected by switches.

II. MODELLING

Basic building blocks for the delta sigma capacitance to digital modulator (CDM) have been described in VHDL-AMS, like capacitors, switches, operational transconductance amplifiers (OTA), comparators and digital blocks. For the OTA for example two different models were implemented. The first was based on an equivalent circuit show in Figure 2 and the second model on a Laplace transfer function. The original transistor model was a BSIM3V3.
The implementation of the first stage of the differential OTA is shown in the following as a short example of the VHDL-AMS code.

```vhdl-ams
I_IN1p == -gm*(V_IN-Offset);
I_IN1n == -gm*(V_IN-Offset);
if (domain = quiescent_domain) use
  c1_p_charg == C1 * 0.0;
  c1_n_charg == C1 * 0.0;
  I_C1P == 0.0;
  I_C1N == 0.0;
else
  c1_p_charg == C1 * V_EL1p;
  c1_n_charg == C1 * V_EL1n;
  I_C1P == c1_p_charg'dot;
  I_C1N == c1_n_charg'dot;
end use;
I_R1p == V_EL1P/R1;
I_R1n == V_EL1n/R1;
```

In the same way the output current of the OTA is finally modelled as a function of the input voltage. Output current limitation was achieved by a tangens hyperbolicus function. Figure 3 shows a comparison of the simulated OTA open loop transfer function for the AMS- and the BSIM3V3- models.

To compare the simulation time for the different models the same transient simulation was set up with two different AMS-simulators, namely SIMPLORER from ANSOFT cooperation and the AMS-Designer from CADENCE. As reference SPECTRE, also from CADENCE was used. Transient simulations with the AMS- models were faster by a factor of about 40 times compared to SPECTRE simulations in conservative mode.

Using the developed AMS models the circuit of Figure 1 was implemented and compared with a transistor based implementation. Two different models for the switches were used, an ideal one with fixed on- and off- resistance and a real one with a fitted timing behaviour.

Signal quantization noise ratio (SQNR) and the calculated effective numbers of bits (ENOB) are used to assess the quality of the modulators. Therefore a large number of conversions must be simulated to calculate the Power Spectral Density (PSD) by a DFT and to derive the ENOBs.
The increase of simulation speed by a factor higher than 500 times for the model with ideal switches and still 320 times with real switches in figure 5 shows the enormous advantage of the AMS-modelling. The improvement in simulation speed however has an impact on the simulation accuracy. The result of the MATLAB model in Figure 6 shows the maximum theoretical value of the SQNR = 81.2 dB, which may be achieved by this circuit. The SQNR degrades step by step whenever more parts of the circuit are replaced by non ideal blocks with a final SQNR = 68.7 dB for the simulation on transistor level. Therefore the AMS models should be used for the evaluation of new architectures and for the exploration of the design space. For the final high accuracy simulation precise transistor models are still necessary.

III. IMPLEMENTATION

A. Higher Order Modulators

The block diagram of a second order CDM is shown in figure 10 with a cascade of integrators with feedback to the first and the second stage (CIFB).

![Fig. 10: Block diagram of a second order CDM](image-url)
A fourth order CDM structure is depicted in Figure 11. It is based on a MASH 2-2 architecture.

For the test chip implementation only the analogue parts were integrated. The digital correction circuit was designed on an FPGA.

B. Noise Analysis

Disregarding flicker noise, the resolution of a Delta Sigma Modulator (DSM) in Switched Capacitor (SC) technology is mainly limited by the kT/C - noise on the switched capacitors, which results from the thermal noise of the switch resistors /1/. Therefore, large sampling capacitors are desirable. In a capacitive sensor interfacing scheme however, where the sensor capacitance directly serves as sampling capacitor, small frontend capacitors are desirable to increase the signal gain /2/. Despite the increased influence of the thermal noise, a higher signal-to-noise ratio (SNR) can be achieved using smaller capacitors.

The noise contributions of the second and subsequent integrators are neglected in this noise analysis, since the overall noise budget is dominated by the first integrator. In the following, thermal and flicker noise of the first integrator stage are considered. The thermal noise of the switches is sampled on the feedback capacitor C\textsubscript{fb1}, the sensor capacitor C\textsubscript{sens}, and the parasitic capacitor C\textsubscript{para}/2. C\textsubscript{para} is the sum of the sensor and circuit parasitics at the sensor interface. The sampling through the switches results in kT/C - noise contributions with mean square noise voltages of kT/C\textsubscript{fb1}, kT/C\textsubscript{sens}, and kT/C\textsubscript{para}/2 on the capacitors respectively.

The thermal noise and the flicker noise of the main contributing input transistors of the op-amp, a total mean square noise voltage \( V_{\text{out,noise}}^2 \) at the output or on the feedback capacitor of the first integrator according to (Equ. 1) results. \( f_1 \) is the lowest frequency of interest and \( f_s/(2\text{OSR}) \) is the signal bandwidth. \( f_s \) is the sampling frequency and \( y \) (Equ. 4) is the op-amp factor with the switch on-resistance \text{R}_{\text{on}} \) and the transconductance \text{g}_\text{m1} \) of the op-amp input transistors. In 4kT/C, a factor of 2 is caused by switching in both, the sampling phase \( \phi_1 \) and the integration phase \( \phi_2 \). A second factor of 2 results from the differential design, where uncorrelated noise from the n- and p-side sampling capacitors are added /3|4/. \( H_{\text{thermal}} \) (Equ. 2) is the thermal noise transfer factor, given by the square root of the ratio of the input capacitances to the feedback capacitance plus the transfer factor of the feedback capacitance itself.

The flicker noise of the first integrator stage is expressed by the flicker noise of the noise-equivalent transistors at the input of the op-amp. W and L are the width and length of the op-amp noise-equivalent transistors. \( K_{\text{flicker}} \) is the flicker noise coefficient, which is a process constant, and \( C'\text{ox} \) is the specific oxide capacitance per unit area of the transistors. \( H_{\text{flicker}} \) (Equ. 3) is the flicker noise transfer factor, which depends on the integration capacitance \( C_{\text{f1}} \) and the feedback capacitance \( C_{\text{fb1}} \) of the first integrator.

\[
V_{\text{out,noise}}^2 = \left| H_{\text{thermal}} \right|^2 \cdot \frac{4kT}{C_{\text{fb1}} \cdot \text{OSR}} \cdot y + \left| H_{\text{flicker}} \right|^2 \cdot \frac{2 \cdot K_{\text{flicker}}}{C'\text{ox} \cdot W \cdot L} \cdot \ln \frac{f_s}{f_1} \quad \text{Equ. 1}
\]

with

\[
\left| H_{\text{thermal}} \right| = \sqrt{1 + \frac{C_{\text{sens}} + \frac{C_{\text{para}}}{2}}{C_{\text{fb1}}}} \quad \text{Equ. 2}
\]

\[
\left| H_{\text{flicker}} \right| = \frac{1 + \frac{C_{\text{fb1}}}{C_{\text{f1}}}}{C_{\text{fb1}}} \quad \text{Equ. 3}
\]

\[
y = 1 + \frac{1}{6(1+2R_{\text{on}}y_{\text{unc}})} \quad \text{Equ. 4}
\]

\( y \) can be omitted for \( 2R_{\text{on}}y_{\text{unc}} \gg 1 \).

\[ V_{\text{out,signal}} = V_{\text{ref}} \cdot \frac{\Delta C_{\text{sens}}}{C_{\text{f1}}} \quad \text{Equ. 5} \]

\[ \text{SNR}_{\text{thermal}} = \frac{V_{\text{ref}}^2 \cdot \Delta C_{\text{sens}}^2 \cdot \text{OSR}}{4kT \left( C_{\text{f1}} + \frac{C_{\text{sens}} + \frac{C_{\text{para}}}{2}}{2} \right) \cdot y} \quad \text{Equ. 6} \]

The signal-to-noise ratio is given by the square of the signal voltage \( V_{\text{out,signal}} \) at the output according to (Equ. 5) divided by \( V_{\text{out,noise}}^2 \). \( V_{\text{ref}} \) is the reference voltage of the sensor capacitors and \( \Delta C_{\text{sens}} \) is the sensor capacitance variation to be measured. Flicker noise can be modulated out of the signal frequency band hence the thermal noise becomes dominant. Neglecting flicker noise, the thermal noise dependent SNR in (Equ. 6) is obtained. The resolution can be increased by reducing the feedback, sensor, and parasitic capacitances for a constant sensor signal charge, OSR and reference voltage.
C. Input stage

Figure 11 shows an input structure for a fully differential input stage. Sensor and reference capacitor should be carefully layouted and located close to each other in order to minimise parasitic influences. On the test chip two parallel channels have been implemented for each type of modulator.

$C_{\text{sens}}$ and $C_{\text{ref}}$ are connected in a differential configuration, where $C_{\text{sens}}$ is the sensor capacitor and $C_{\text{ref}}$ is the reference capacitor. During clock phase $\phi_1$, the capacitors are charged to $V_{\text{ref}+} - V_{\text{ref}-}$. During clock phase $\phi_2$, the difference sensor discharge $Q_{\text{sens}} - Q_{\text{ref}}$ is applied to the integrator.

A folded-cascode operational transconductance amplifier (OTA) is used in this design with an n-channel input stage in order to benefit from the lower white noise level compared to p-channel transistors. The input transistors are large to reduce the flicker noise. The common-mode feedback of the amplifiers is realised in switched-capacitor technique. The OTAs have an open-loop gain of 70 dB, a gainbandwidth product of 200 MHz and a slew-rate of 14 V/\mu s in order to allow sufficient settling in the sampling phases. The integrated capacitors are of polysilicon-to-polysilicon type placed on a grounded n-well. For range selection, the feedback capacitors $C_{\text{fb}}$ and the integration capacitors $C_{\text{f}}$ of the first integrator are adjustable in four steps, from 60 fF to 240 fF for $C_{\text{fb}}$ and from 120 fF to 480 fF for $C_{\text{f}}$. The second and the following integrator stages have values of $C_{\text{fb}}=100$ fF and $C_{\text{f}}=200$ fF.

IV. EXPERIMENTAL RESULTS

The test chip is characterised on a custom printed circuit board in a CQFP44 package. The single-bit modulator output data stream is analysed in the frequency domain using a 128kS FFT with a Hanning window. The SNR is calculated by integrating the power spectral density (PSD) over the signal bandwidth. The noise level is 0.2 aF/sqrt(Hz) for the 2nd order modulator and 0.52 aF/sqrt(Hz) for the 4th order modulator. The peak SNR is measured on a configuration with the lowest gain setting of the first integrator, which gives a larger full-scale range. The full-scale capacitive range is quantified statically for lack of adequate dynamic test equipment. The results of the noise simulations and measurements for the second order are shown in figure 12 and for the fourth order in figure 13.

![Fig. 11: Block diagram of the differential input stage with sensor and reference capacitor](image1)

![Fig. 12: Block diagram of the differential input stage with sensor and reference capacitor](image2)
The noise bandwidth (NBW) is the normalised unit bandwidth used for the FFT scaling. The plots display the product of the noise density and the noise bandwidth. The calculated resolution (Equ. 6) is 5.1 aF if only thermal noise is considered and 9.5 aF if flicker noise is included. The measured value of 19.3 aF includes additional contributions caused by circuit non-idealities and noise from the references and the measurement environment.

A picture of the test chip is shown in figure 14. Two parallel channels are implemented for the second order and also for the fourth order modulator. The test chip was integrated on the 350nm DPTM CMOS technology C35B3C0 of austriamicrosystems AG. Onchip capacitors were implemented as poly-poly structures.

![chip photo](image)

Fig. 14: Chip photo of the test chip with second and fourth order CDM

### Table 1: Summary of Test Chip Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>2. order CDM</th>
<th>4. order CDM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>3.3V</td>
<td>3.3V</td>
</tr>
<tr>
<td>Sampling Freq</td>
<td>10 MHz</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Oversampling Ratio</td>
<td>500</td>
<td>50</td>
</tr>
<tr>
<td>SNR&lt;sub&gt;max&lt;/sub&gt; (BW=10kHz)</td>
<td>73.4 dB</td>
<td>66.8 dB</td>
</tr>
<tr>
<td>Resolution (Cap)</td>
<td>19.3 aF</td>
<td>51.3 aF</td>
</tr>
<tr>
<td>Power consumption</td>
<td>64 mW</td>
<td>116 mW</td>
</tr>
</tbody>
</table>

Table 1 summarize the results for the test chip. The lower SNR of the 4th order modulator is caused by the lower oversampling ratio. Theoretically the SNR of the 2nd order CDM working with a 10 times higher OSR should be 10dB higher than the result of the 4th order. Since we only measured 6.6 dB more we assume that the noise in the test environment, especially in the reference voltages caused this additional measurement loss. Current consumption for both modulators is quite high but significant reduction can be achieved by optimization of the operational transconductance amplifiers.

V. CONCLUSIONS

Capacitance to digital converters based on delta sigma modulators offer a good solution for capacitive sensor signal acquisition with high resolution. Using VHDL-AMS models in the architectural design phase overcome the problem of long simulation times for this kind of measurement principle with high oversampling ratios. So for a first order capacitive to digital modulator the time for a simulation run was reduced by a factor of up to 500 times when AMS models were used.

To explore the achievable resolution for this kind of capacitive measurement a second order CIFB structure were implemented in a 350nm CMOS technology. Sampling clock is 10 MHz. The noise optimized circuit yields a noise level of 0.2 aF/sqrt(Hz) at an OSR of 500, compared to 1.5 aF/sqrt(Hz) given for the 2nd order CDC in [2]. A fourth order MASH2-2 structure was also implemented for a reduced sampling clock of 1MHz and an OSR of 50. The noise level for this circuit was measured at 0.52 aF/sqrt(Hz).

Calculations and transistor-level simulations of the thermal and flicker noise contributions have been performed and are in good agreement with the measured results. Power dissipation of the circuits can be improved, mainly for the 2nd, 3rd and 4th integrators due to the noise shaping characteristic of the modulator. Using correlated double sampling (CDS) will further reduce the flicker noise and the offset drift of the OTAs. This will result in a SNR limited by kT/C-noise.

A further advantage of the CDM in switched capacitor technique is the easy implementation of offset compensation. Using an integrated capacitive DAC instead of a single reference capacitor it is also possible to implement a digital auto calibration. In a similar way different gain stages can be implemented by splitting the integration or feedback capacitor.

REFERENCES


